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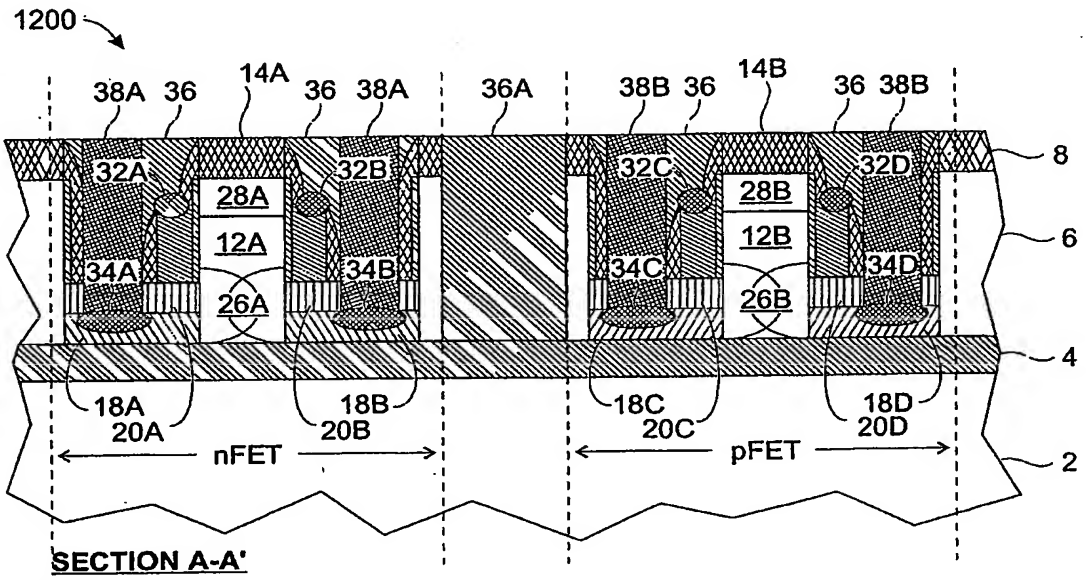
(54) Title: VERTICAL FIN-FET MOS DEVICES



(57) Abstract: A new class of high-density, vertical Fin-FET devices that exhibit low contact resistance is described. These vertical Fin-FET devices have vertical silicon "fins" (12A) that act as the transistor body. Doped source and drain regions (26A, 28A) are formed at the bottoms and tops, respectively, of the fins (12A). Gates (24A, 24B) are formed along sidewalls of the fins. Current flows vertically through the fins (12A) between the source and drain regions (26A, 28A) when an appropriate bias is applied to the gates (24A, 24B). An integrated process for forming pFET, nFET, multi-fin, single-fin, multi-gate and double-gate vertical Fin-FETs simultaneously is described.

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